1) Consider the CMOS inverter circuit in Figure P1 with the following parameters. Assume long channel transistors and no velocity saturation.

V_{DD}=3.3V;
k_n=200μA/V²;
k_p=80μA/V²;
V_{T0n}=0.6V;
V_{T0p}=-0.7V;

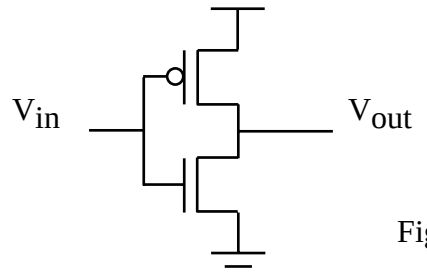

Figure P1

Find V_{OL}, V_{OH}, V_{IL}, and V_{IH} on the VTC. Also find the noise margins of this inverter.

Solution:

V_{OH} and V_{OL}: For a CMOS inverter $V_{OH}=V_{DD}=3.3V$ and $V_{OL}=0V$.

V_{IL}: By definition, V_{IL} is the smaller of the two input voltage values at which the slope of the VTC becomes equal to (-1), i.e. $dV_{out}/dV_{in}=-1$. In this case nMOS transistor is in saturation while the pMOS transistor is in linear mode. From $I_{D,n}=I_{D,p}$ we obtain:

$$\frac{k_n}{2}\left(V_{GS,n}-V_{T0,n}\right)^2=\frac{k_p}{2}\left[2\left(V_{GS,p}-V_{T0,p}\right)V_{DS,p}-V_{DS,p}^2\right] \qquad (3.1)$$

Note that $V_{GS,n}=V_{in}$, $V_{DS,n}=V_{out}$, $V_{GS,p}=-\left(V_{DD}-V_{in}\right)$, and $V_{DS,p}=-\left(V_{DD}-V_{out}\right)$. Substituting these expressions into (3.1) yields:

$$\frac{k_n}{2}\left(V_{in}-V_{T0,n}\right)^2=\frac{k_p}{2}\left[2\left(V_{in}-V_{DD}-V_{T0,p}\right)\left(V_{out}-V_{DD}\right)-\left(V_{out}-V_{DD}\right)^2\right] \qquad (3.2)$$

To satisfy $dV_{out}/dV_{in}=-1$, we differentiate both sides of (3.2):

$$k_n\left(V_{in}-V_{T0,n}\right)=k_p\left[\left(V_{in}-V_{DD}-V_{T0,p}\right)\left(\frac{dV_{out}}{dV_{in}}\right)+\left(V_{out}-V_{DD}\right)-\left(V_{out}-V_{DD}\right)\left(\frac{dV_{out}}{dV_{in}}\right)\right] \qquad (3.3)$$

Substituting $V_{in}=V_{IL}$ and $dV_{out}/dV_{in}=-1$ into(3.3), we obtain:

$$k_n\left(V_{IL}-V_{T0,n}\right)=k_p\left(2V_{out}-V_{IL}+V_{T0,p}-V_{DD}\right) \qquad (3.4)$$

Then V_{IL} as a function of V_{out} can be expressed as:

$$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}}{1 + k_R} \tag{3.5}$$

where

$$k_R = k_n / k_p \tag{3.6}$$

Substituting values into (3.5) produces

$$V_{IL} = 0.57V_{out} - 0.71 \tag{3.7}$$

Now substituting this expression into(3.2) results in:

$$0.66V_{out}^2 + 0.05V_{out} - 6.65 = 0 \tag{3.8}$$

The only root that gives a physically correct solution for V_{out} is V_{out}=3.14V. Substitute V_{out}=3.14V into (3.7) produces:

V_{IL}=1.08V.

a) V_{IH}: In this point nMOS is in linear mode and pMOS in saturation. Similarly to VIL we apply KCL to the output node:

$$\frac{k_n}{2}\left[2\left(V_{GS,n} - V_{T0,n}\right)V_{DS,n} - V_{DS,n}^2\right] = \frac{k_p}{2}\left(V_{GS,p} - V_{T0,p}\right)^2 \tag{3.9}$$

Again, using $V_{GS,n} = V_{in}$, $V_{DS,n} = V_{out}$, $V_{GS,p} = -\left(V_{DD} - V_{in}\right)$, and $V_{DS,p} = -\left(V_{DD} - V_{out}\right)$, (3.9) can be rewritten as:

$$\frac{k_n}{2}\left[2\left(V_{in} - V_{T0,n}\right)V_{out} - V_{out}^2\right] = \frac{k_p}{2}\left(V_{in} - V_{DD} - V_{T0,p}\right)^2 \tag{3.10}$$

Differentiating both sides with respect to V_{in}:

$$k_n\left[\left(V_{in} - V_{T0,n}\right)\left(\frac{dV_{out}}{dV_{in}}\right) + V_{out} - V_{out}\left(\frac{dV_{out}}{dV_{in}}\right)\right] = k_p\left(V_{in} - V_{DD} - V_{T0,p}\right) \tag{3.11}$$

Substituting $V_{in} = V_{IL}$ and $dV_{out}/dV_{in} = -1$ into(3.11), we obtain:

$$k_n\left(-V_{IH} + V_{T0,n} + 2V_{out}\right) = k_p\left(V_{IH} - V_{DD} - V_{T0,p}\right) \tag{3.12}$$

Then V_{IH} as a function of V_{out} can be expressed as:

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + k_R\left(2V_{out} + V_{T0,n}\right)}{1 + k_R} \tag{3.13}$$

Substituting values into (3.13) produces:

$$V_{IH} = 1.43V_{out} + 1.17$$

Next, substitute this expression into the KCL equation (3.10) to obtain a second-order polynomial in V_{out}:

$$2.5\left[2(1.43V_{out} + 1.17 - 0.6)V_{out} - V_{out}^2\right] = (1.43V_{out} - 1.43)^2 \quad (3.14)$$

$$2.61V_{out}^2 + 6.94V_{out} - 2.04 = 0 \quad (3.15)$$

The only root that gives a physically correct solution for V_{out} is V_{out}=0.27V/

For this value we calculate the V_{IH} as:

$$V_{IH} = 1.43 \cdot 0.37 + 1.17 = 1.55V \quad (3.16)$$

Finally, the noise margins are:

$$NM_L = V_{IL} - V_{OL} = 1.08V \quad (3.17)$$

$$NM_H = V_{OH} - V_{IH} = 1.75V \quad (3.18)$$

---

2) Consider a CMOS inverter circuit with power supply voltage V_{DD} = 3.3V. The I-V characteristic of the NMOS transistor is specified below. When V_{GS}=3.3V, the drain current reaches its saturation level I_{sat} = 2mA, for V_{DS} > 2.5V. Assume that the input signal applied to the gate is a step pulse that switches instantaneously, from 0V to 3.3V.

V_{DD}=3.3V;

I_{sat}=2mA (for V_{DS}>2.5V and V_{GS}=3.3V);

C_{load}=300fF.

Find: t_{delay} necessary for the output to fall from 3.3V to 1.65V ($V_{DD}/2$).

Solution:

We will assume that the NMOS transistor operates in saturation from t=0 to t=t_{sat} and it will operate in linear region from t=t_{sat} to t=t_{delay}. Since 3.3-2.5=0.8, V_{Tn}=0.8V;

The current equation for the saturation region can be written as:

$$C\frac{dV_{out}}{dt} = -I_D = -I_{sat} = -\frac{1}{2}k_n\left(V_{OH} - V_{T,n}\right)^2 \quad (4.1)$$

We can calculate the amount of time in which the nMOS transistor operates in saturation (t_{sat}) by integrating this equation.

$$\int_{t=0}^{t=t_{sat}} dt = -\int_{V_{out}=3.3V}^{V_{out}=2.5V} \frac{C}{I_D} dV_{out} \quad (4.2)$$

$$t_{sat} = \frac{V_{T,n} C}{I_{sat}} = \frac{0.8V \cdot 300fF}{2mA} = 120ps \tag{4.3}$$

The transconductance k_n of the nMOS transistor can be found as follows:

$$k_n = \frac{2I_{sat}}{\left(V_{OH} - V_{T,n}\right)^2} = \frac{2 \cdot 2 \cdot 10^{-3}}{\left(3.3 - 0.8\right)^2} = 0.64 \cdot 10^{-3} \frac{A}{V^2} \tag{4.4}$$

Now, the current equation for the linear region:

$$C\frac{dV_{out}}{dt} = -I_D = -\frac{1}{2} k_n \left[2\left(V_{OH} - V_{T,n}\right)V_{out} - V_{out}^2\right] \tag{4.5}$$

Integrating (4.5) from 2.5V to 1.65V, for linear region we have:

$$\int_{t=t_{sat}}^{t=t_{delay}} dt = -2C \int_{V_{out}=2.5V}^{V_{out}=1.65V} \frac{dV_{out}}{k_n \left[2\left(V_{OH} - V_{T,n}\right)V_{out} - V_{out}^2\right]} \tag{4.6}$$

$$t_{delay} - t_{sat} = -\frac{C}{k_n} \frac{1}{\left(V_{OH} - V_{T,n}\right)} \ln\left(\frac{V_{out}}{2\left(V_{OH} - V_{T,n}\right) - V_{out}}\right)_{V_{out}=2.5}^{V_{out}=1.65} =$$

$$= \frac{C}{k_n} \frac{1}{\left(V_{OH} - V_{T,n}\right)} \left[\ln\left(\frac{2\left(V_{OH} - V_{T,n}\right) - V_{1.65}}{V_{1.65}}\right) - \ln\left(\frac{2\left(V_{OH} - V_{T,n}\right) - V_{2.5}}{V_{2.5}}\right)\right] = \tag{4.7}$$

$$= \frac{0.3 \times 10^{-12}}{0.64 \times 10^{-3}} \frac{1}{\left(3.3 - 0.8\right)} \left[\ln\left(\frac{2\left(3.3 - 0.8\right) - 1.65}{1.65}\right) - \ln\left(\frac{2\left(3.3 - 0.8\right) - 2.5}{2.5}\right)\right] = 133ps$$

Thus, the total delay time is:

$$t_{delay} = 120 + 133 = 253ps \tag{4.8}$$

Note that t_{delay} corresponds to the propagation delay τ_{pHL} for falling output.

---

3) Consider a CMOS inverter with supply voltage of V_{DD} = 5V. Assume long channel transistors and no velocity saturation. Determine the fall time t_{fall}, defined as the time elapsed between 90% to 10% transition of the output voltage. Assume $k_n' = 20\mu A/V^2$, others are given below.

V_{DD}=5V;

k_p'=80μA/V^2;

W/L=10;

V_{T0n}=1.0V;

C_{load}=1pF.

Find: τ_{fall} (from $V_{out}|_{90\%}$ =4.5V to $V_{out}|_{10\%}$=0.5V)

Solution:

Average current method

The average capacitor current during the discharge is:

$$I_{avg} = \frac{1}{2}\left[I\left(V_{in} = 5V, V_{out} = 4.5V\right) + I\left(V_{in} = 5V, V_{out} = 0.5V\right)\right] =$$

$$= \frac{1}{2}\left[\frac{1}{2}k_n\left(V_{in} - V_{T,n}\right)^2 + \frac{1}{2}k_n\left(2\left(V_{in} - V_{T,n}\right)V_{out} - V_{out}^2\right)\right] =$$

$$= \frac{1}{2}\cdot\frac{1}{2}\cdot 20\times10^{-6}\cdot 10\left[(5-1)^2 + \left(2(5-1)0.5 - 0.5^2\right)\right] = 0.9875mA$$

The fall time is then found as:

$$\tau_{fall} = \frac{C\cdot\Delta V}{I_{avg}} = \frac{1\times10^{-12}(4.5-0.5)}{0.9875\times10^{-3}} = 4.05\times10^{-9}s = 4.05ns$$

---

4) An inverter is simulated in SPICE in the following conditions and characteristics

SPICE simulation results

a) V_{DD}=1.5V, t_{pHL}=51.13ps, t_{pLH}=71.82ps, I_{av}=15.28μA;

b) V_{DD}=1.2V, t_{pHL}=74.4ps, t_{pLH}=66.46ps, I_{av}=11.99μA.

Find: t_p, power dissipation and PDP and comment on the effect of the power supply reduction on the delay, power and PDP.

Solution:

Case (a):

The propagation delay is given by:

$$t_p = \frac{t_{pLH} + t_{pHL}}{2} = 61.47ps$$

The DC power dissipation is given by:

$$P = V_{DD}\cdot I_{av} = 1.5V\cdot 15.28\mu A = 22.92\mu W$$

The Power Delay Product (PDP) is given by:

$$PDP = P\cdot t_p = 1.408fJ$$

Case (b):

The propagation delay is given by:

$$t_p = \frac{t_{pLH} + t_{pHL}}{2} = 70.43\,ps$$

The DC power dissipation is given by:

$$P = V_{DD} \cdot I_{av} = 1.2V \cdot 11.99\mu A = 14.39\mu W$$

The Power Delay Product (PDP) is given by:

$$PDP = P \cdot t_p = 1.01\,fJ$$

Comment: When the power supply voltage is reduced:

a) t_p increases due to the reduction in transistor drive

b) P reduces

c) PDP reduces since the % decrease in power dissipation offsets the increase in t_p.

---

5) For the resistive-load inverter in Figure P5, and assume an output load of 3 pF
Given: V_{T0} = 0.43V, V_{DSAT}=0.63, k'$_n$=115μA/V^2, λ = 0.06 V^{-1}, V_{OH} = 2.5V, V_{OL} = 0.0463V

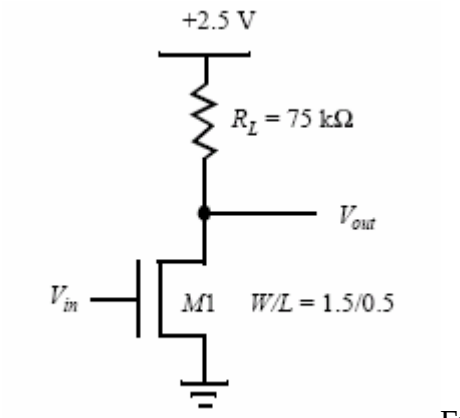

Figure P5

a) Calculate *tplh*, *tphl*, and *tp*

Solution

t_{pLH}=0.69$R_L C_L$= 155 nsec.

For t_{pHL}: First calculate R_{on} for V_{out} at 2.5V and 1.27315V ← (V_{OH} – V_{OL})/2.
At V_{out}=2.5V, I_{DVsat}=0.439mA giving R_{on}= 5695Ω

At V_{out}=1.27315V, I_{Dvsat}=0.4106mA giving R_{on}= 3100.85Ω.
Thus, the average resistance between V_{out}=2.5V and V_{out}=1.27315V is $R_{average}$=4.398kΩ.
$t_{pHL}=0.69R_{average}C_L$=9.104nsec.
t_p=av{t_{pLH}, t_{pHL}}=82.05nsec

ASIDE: if first-order approximation is considered, such that the 50% point is $V_{dd}/2$

At V_{out}=1.25V, I_{Dvsat}=0.41m giving R_{on}= 3049Ω.
Thus, the average resistance between V_{out}=2.5V and V_{out}=1.25V is $R_{average}$=4.372kΩ.
$t_{pHL}=0.69R_{average}C_L$=9.05nsec.
t_p=av{t_{pLH}, t_{pHL}}=82.0nsec

b) Are the rising and falling delays equal? Why or why not?

Solution
t_{pLH} >> t_{pHL} because R_L=75kΩ is much larger than the effective linearized on-resistance of M1.

c) Compute the static and dynamic power dissipation assuming the gate is clocked as fast as possible.

Solution
Static Power:

$V_{IN}=V_{OL}$ gives $V_{out}=V_{OH}$=2.5V, thus I_{VDD}=0A so P_{VDD}=0W.
$V_{IN}=V_{OH}$ gives $V_{out}=V_{OL}$=46.3mV, which is in the linear region.
Calculating the current through M1 gives I_{VDD}=32.8μA → P_{VDD}=82μW

Dynamic Power: *NOTE:* $f_{max}= 1 / t_p =1 / 82.0nsec$

$P_{dyn}=C_L\Delta V*V_{dd}*f_{max}$=3pF*(2.5V-46.3mV)*2.5V*12.2MHz=0.225mW.

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6) Figure P6 shows two implementations of MOS inverters. Circuit A uses only NMOS transistors. Circuit B is a static CMOS inverter (NOTE: short-channel transistors and velocity saturated)

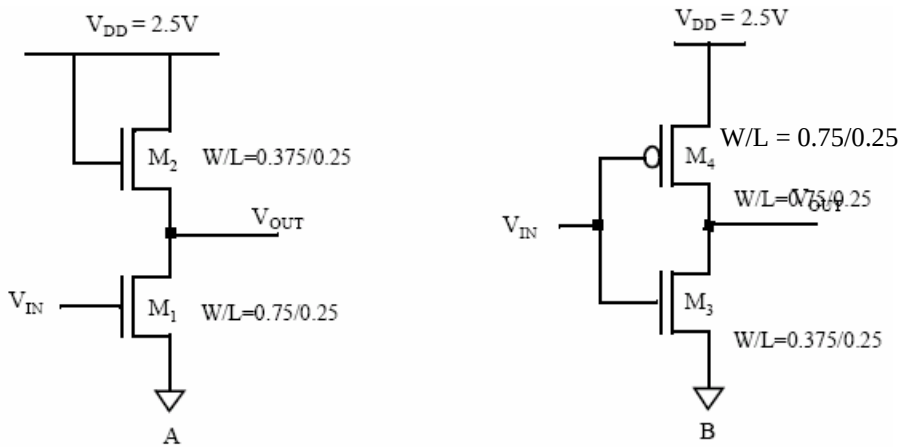

Figure P6

a) Calculate V_{OH}, V_{OL}, V_M for each case.

Solution

Circuit A.

V_{OH}: We calculate V_{OH}, when M1 is off. The threshold for M2 is:

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right),\ V_{SB} = V_{OUT},\ \left|-2\phi_F\right| = 0.6V$$

and M2 will be off when: $V_{GS} - V_T = V_{DD} - V_{OUT} - V_T = 0$,

Substitute V_T in the last equation and solve for V_{OUT}.

$$V_{DD} - V_{OUT} - V_T = 2.5 - V_{OUT} - (0.43 + 0.4 \cdot (\sqrt{\left|0.6 + V_{OUT}\right|} - \sqrt{\left|0.6\right|})) = 0$$

We get **V_{OUT}=V_{OH}=1.765V**

V_{OL}: To calculate V_{OL}, we set V_{IN}=V_{DD}=2.5V.

We expect V_{OUT} to be low, so we can make the assumption that M2 will be velocity saturated and M1 will be in the linear region.

For M2: $I_{D2} = k_n \cdot \frac{W_2}{L_2} \cdot \left((V_{GS} - V_T) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}\right) \cdot (1 + \lambda V_{DS})$ and

for M1: $I_{D1} = k_n \cdot \frac{W_1}{L_1} \cdot \left((V_{GS} - V_{T0}) \cdot V_{DS} - \frac{V_{DS}^2}{2}\right)$

Setting $I_{D1} = I_{D2}$, we get an equation and we solve for V_{OUT}.

We get: **V_{OUT}=V_{OL}=0.263V**, so our assumption holds.

V_M: To calculate V_M we set V_M=V_{IN}=V_{OUT}.

Assuming that both transistors are velocity saturated, then we have the next pair of equations:

$$I_{D1} = k_n \cdot \frac{W_1}{L_1} \cdot \left((V_M - V_{T0}) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}\right) \cdot (1 + \lambda V_M)$$

$$I_{D2} = k_n \cdot \frac{W_2}{L_2} \cdot \left((V_{DD} - V_M - V_T) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}\right) \cdot (1 + \lambda (V_{DD} - V_M))$$

Setting $I_{D1} = I_{D2}$, we get for **V_M = 1.269V**

Circuit B.

When V_{IN}=0V, the NMOS transistor is off and the PMOS transistor in on and pulls V_{OUT} up to V_{DD}, so **V_{OH}=2.5**. Similarly, when V_{IN}=2.5V, the PMOS transistor is off and the NMOS transistor pulls V_{OUT} all the way down to ground, so V_{OL}=0V.

To calculate V_M we set V_M=V_{IN}=V_{OUT}.

We assume that both transistors are velocity saturated. We get the following pair of equations.

$$I_{D4} = k'_p \cdot \frac{W_4}{L_4} \cdot \left((V_M - V_{DD} - V_{T0p}) \cdot V_{DSATp} - \frac{V_{DSATp}^2}{2} \right) \cdot (1 + \lambda_p V_M)$$

$$I_{D3} = k'_n \cdot \frac{W_3}{L_3} \cdot \left((V_M - V_{T0n}) \cdot V_{DSATn} - \frac{V_{DSATn}^2}{2} \right) \cdot (1 + \lambda_n V_M)$$

Setting $I_{D3} + I_{D4} = 0$, we get V_M = **1.095V**.
So the assumption that both transistors were velocity saturated holds.

b) Find V_{IH}, V_{IL}, N_{ML} and N_{MH} for each inverter and comment on the results. Given that V_{IL} = 0.503V and V_{IH} = 1.35V for circuit A, and V_{IL} = 0.861V and V_{IH} = 1.22V for circuit B. How can you increase the noise margins and reduce the undefined region?

Solution
Circuit A
Based on the V_{OL} and V_{OH} from part (a)
V_{IL} = 0.503V, V_{IH} = 1.35V
$N_{MH} = V_{OH} - V_{IH}$ = 1.765 - 1.35 = 0.415V, $N_{ML} = V_{IL} - V_{OL}$ = 0.503- 0.263 = 0.240V
Circuit B
V_{IL} = 0.861V, V_{IH} = 1.22V
$N_{MH} = V_{OH} - V_{IH}$ = 2.5V - 1.22V = 1.28V, $N_{ML} = V_{IL} - V_{OL}$ = 0.861V- 0V = 0.861V
We can increase the noise margins by moving V_M closer to the middle of the output voltage swing.

c) Comment on the differences in the VTCs, robustness and regeneration of each inverter.

Solution
It is clear from the two VTCs, that the CMOS inverter is more robust, since the low and high noise margins are higher than the first inverter. Also the regeneration in the second inverter is greater since it provides rail to rail output and the gain of the inverter is much greater.

---

7) For this problem assume:
V_{DD} = 2.5V, W_P/L = 1.25/0.25, W_N/L = 0.375/0.25, $L=L_{eff}$ =0.25μm (i.e. x_d= 0μm), $C_L=C_{invgate}$, k_n' = 115μA/V^2, k_p'= -30μA/V^2, V_{tn0} = | V_{tp0} | = 0.4V, λ= 0V^{-1}, γ = 0.4, 2|ϕ_f|=0.6V, and t_{ox} = 58A. Use the HSPICE model parameters for parasitic capacitance given below (i.e. C_{gd0}, C_j, C_{jsw}), and assume that V_{SB}=0V. (NOTE: short-channel transistors and velocity saturated)

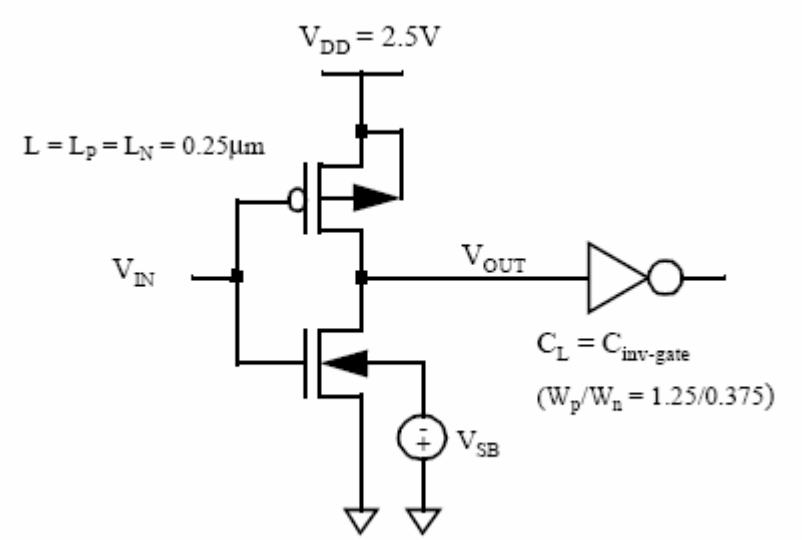

Figure P7

Parasitic Capacitance Parameters (F/m)##
NMOS: CGDO=$3.11\text{x}10^{-10}$, CGSO=$3.11\text{x}10^{-10}$, CJ=$2.02\text{x}10^{-3}$, CJSW=$2.75\text{x}10^{-10}$
PMOS: CGDO=$2.68\text{x}10^{-10}$, CGSO=$2.68\text{x}10^{-10}$, CJ=$1.93\text{x}10^{-3}$, CJSW=$2.23\text{x}10^{-10}$

a) What is the V_M for this inverter?

Solution
Assume that V_M is around midrail (1.25V). That means that the NMOS is velocity saturated and the PMOS is saturated. To find V_M, we set the sum of the currents at V_{out} equal to 0 using the correct equation for each device:

$$k_n \cdot V_{DSATn} \cdot \left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p \cdot 0.5 \cdot (V_M - V_{DD} - V_{Tp})^2 = 0 .$$

Plug in numbers:

$$172.5 \cdot 0.6 \cdot (V_M - 0.4 - 0.315) + (-150) \cdot 0.5 \cdot (V_M - 2.5 - (-0.4))^2 = 0$$

$$103.5 V_M - 74 - \left(-75 \cdot \left(V_M^2 - 4.2 V_M + 4.41\right)\right) = 0 .$$

Solving this quadratic gives $\boldsymbol{V_M = 1.245}$ **V**.

b) Calculate t_{PHL}, t_{PLH} assuming C_{Leff} = 6.5fF. (Assume an ideal step input, i.e. t_{rise}=t_{fall}=0. Do this part by computing the average current used to charge/discharge C_{Leff}.)

Solution

We can estimate the propagation delay using the approximation $\Delta t = \Delta Q/I$, where ΔQ

$= C_{Leff}V_{DD}$ and I is the average current used to charge/discharge C_{Leff}. During the high-to-low transition C_{Leff} is discharged through the NMOS transistor so $I = I_{avgN}$. During the low-to-high transition C_{Leff} is charged through the PMOS transistor so $I = I_{avgP}$. In summary:

$$t_{delay} \cong \frac{V_{DD} \cdot C_{Leff}}{2 \cdot I_{avg}}, \text{ where}$$

$$I_{avgP} = \frac{I_{ds}(V_o = 0) + I_{ds}\left(V_o = \frac{V_{DD}}{2}\right)}{2}, I_{avgN} = \frac{I_{ds}(V_o = V_{DD}) + I_{ds}\left(V_o = \frac{V_{DD}}{2}\right)}{2}$$

Table 1 shows corresponding values for I_{avgN}, I_{avgP}, t_{PLH}, and t_{PHL}. NOTE- This solution

	V_o (V)	Operation Mode	I_{ds} (mA)	I_{avg} (mA)	Prop Delay (ps)
for t_{PLH}	0	PMOS vel sat.	0.300	0.285	28.5
	1.25	PMOS vel sat	0.270		
for t_{PHL}	2.5	NMOS vel sat.	0.223	0.216	37.65
	1.25	NMOS vel sat	0.208		

included channel length modulation, but it is ok if your solution did not (see problem assumptions).

---

8) Consider the circuit in Figure P8 (which is a low-swing driver, not an inverter).
Given $V_{Tn0} = 0.43$ and $V_{Tp0} = -0.4$. NOTE: short-channel transistors and velocity saturated.

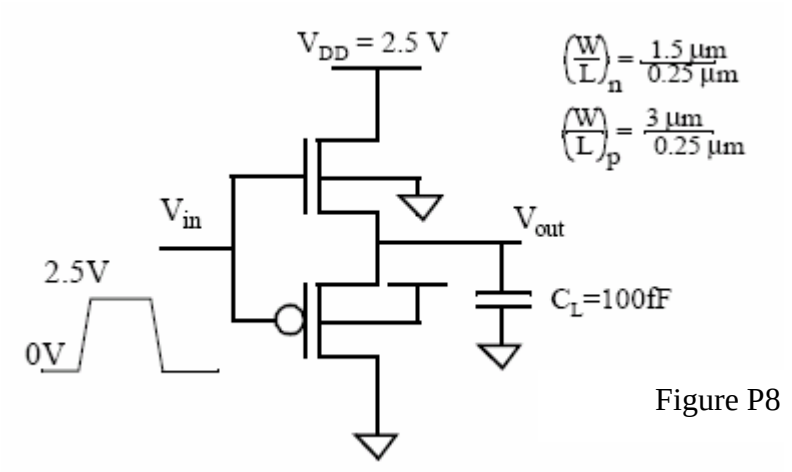

Figure P8

a) What is the voltage swing on the output node (V_{out})? Assume γ=0.

Solution
The range will be from 0.4 V to 2.07 V, since the PMOS is a weak pull down device and the NMOS is a weak pull up device.

b) Compute t_{pLH} (i.e. the time to transition from V_{OL} to $(V_{OH} + V_{OL})$ /2). Assume the input rise time to be 0. V_{OL} is the output voltage with the input at 0V and V_{OH} is the output voltage with the input at 2.5V.

Solution
When the input is high and the capacitor charges, the PMOS device is in cutoff and the NMOS is velocity saturated for the duration of the charging. The total voltage range is 0.4 V to 2.07 V, so the midpoint is 1.24 V. We can use the average current method to approximate t_{plh}. For the velocity saturated NMOS:

$$I = \left(\frac{\mu_n C_{ox} W}{L}\right) V_{DSATN}\left(V_{GS} - V_{tn} - \frac{V_{DSATN}}{2}\right)(1 + \lambda V_{DS})$$

Solving for the current at V=0.4 V and V=1.24 V and averaging yields an average current of 404 uA. Then:

$$t_{plh} = \frac{C\Delta V}{I_{avg}} = \frac{(100fF)(1.24V - 0.4V)}{404uA} = 208ps$$